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EXAMINER	
LI, AIMEE J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/556,473	MANG ET AL.
	Examiner	Art Unit
	Aimee J Li	2183

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 09 August 2004.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 have been considered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-10, 12-19, and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alidina et al., U.S. Patent Number 6,446,193 (herein referred to as Alidina) in view of Gregory T. Byrd and Mark A. Holliday's "Multithreaded Processor Architectures" ©1995 (herein referred to as Byrd).

4. Referring to claim 1, Alidina has taught an accumulation circuit that supports a plurality of threads, comprising:

a. A first operation unit operably coupled to receive a first operand and a second operand corresponding to an operation code issued, wherein the operation unit combines the first and second operands to produce a first operation result (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3)

b. A plurality of accumulation registers operably coupled to the first operation unit, wherein each accumulation register of the plurality of accumulation registers (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3, element 30)

c. A selection block operably coupled to the plurality of accumulation registers and the first operation unit, wherein the selection block selects the second operand provided to the first operation unit from a set of potential operands, wherein the set of potential operands includes contents of each accumulation register of the plurality of accumulation registers (Alidina column 4, lines 63-66 and Figure 3, element SMUX).

d. Wherein a selected accumulation register stores the first operation result (Alidina column 1, line 64 to column 2, line 5)

5. Alidina has not taught multi-threading and having registers and operands which correspond to each individual thread. However, Alidina has taught a digital signal processor specializing in scientific calculations (Alidina column 1, lines 17-28). Byrd has taught multi-threading and having registers and operands which correspond to each individual thread (Byrd pages 38-40). A person of ordinary skill in the art, and as taught in Byrd, would recognize that multi-threading is best suited for scientific and engineering programs (Byrd page 38) and increases the speed and efficiency in the processor by allowing the processor to run other procedures while waiting for a longer background operations, such as accessing slower memory, to complete (Byrd pages 38-40). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multi-threading of Byrd in the device of Alidina to increase speed and decrease processor idle time.

6. Referring to claim 2, Alidina has taught a control block operably coupled to the selection block and the plurality of accumulation registers, wherein the control block receives information based on the operation code and generates control information provided to the plurality of

accumulation registers and the selection block, wherein the control information provided to the plurality of accumulation registers causes the selected accumulation register to store the result when the operation code corresponds to an accumulate operation (Alidina column 5, lines 8-18). Alidina has not taught multi-threading and having registers and operands which correspond to each individual thread. However, Alidina has taught a digital signal processor specializing in scientific calculations (Alidina column 1, lines 17-28). Byrd has taught multi-threading and having registers and operands which correspond to each individual thread (Byrd pages 38-40). A person of ordinary skill in the art, and as taught in Byrd, would recognize that multi-threading is best suited for scientific and engineering programs (Byrd page 38) and increases the speed and efficiency in the processor by allowing the processor to run other procedures while waiting for a longer background operations, such as accessing slower memory, to complete (Byrd pages 38-40). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multi-threading of Byrd in the device of Alidina to increase speed and decrease processor idle time.

7. Referring to claim 3, Alidina has taught wherein when the operation code corresponds to an accumulate operation, the control block provides the control information to the selection block such that the selection block selects a current value stored in the selected accumulation register as the second operand (Alidina columns 1-2, lines 64-5 and Figure 3).

8. Referring to claim 4, Alidina has taught wherein the first operation unit performs an addition operation such that the result of an accumulate operation is a sum of the current value stored in the selected accumulation register and the first operand (Alidina columns 1-2, lines 64-5 and Figure 3).

9. Referring to claim 5, Alidina has taught a second operation unit operably coupled to the first operation unit, wherein the second operation unit is operably coupled to receive a third operand and a fourth operand, wherein the second operation unit combines the third and fourth operands to produce a second operation result, wherein the second operation result is provided to the first operation unit as the first operand (Alidina columns 4-5, lines 26-7 and Figure 3).

10. Referring to claim 6, Alidina has taught wherein the second operation unit performs multiplication operations such that a plurality of multiply and accumulate functions are supported by multi-thread accumulation circuit (Alidina column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3). Alidina has not taught multi-threading and having registers and operands which correspond to each individual thread. However, Alidina has taught a digital signal processor specializing in scientific calculations (Alidina column 1, lines 17-28). Byrd has taught multi-threading and having registers and operands which correspond to each individual thread (Byrd pages 38-40). A person of ordinary skill in the art, and as taught in Byrd, would recognize that multi-threading is best suited for scientific and engineering programs (Byrd page 38) and increases the speed and efficiency in the processor by allowing the processor to run other procedures while waiting for a longer background operations, such as accessing slower memory, to complete (Byrd pages 38-40). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multi-threading of Byrd in the device of Alidina to increase speed and decrease processor idle time.

11. Referring to claim 7, Alidina has not taught an arbitration module operably coupled to the control block and the second operation unit, wherein the arbitration module receives operation codes from a plurality of thread controllers corresponding to the plurality of threads, wherein the

arbitration module determines order of execution of the operation codes received. However, Alidina has taught a digital signal processor specializing in scientific calculations (Alidina column 1, lines 17-28). Byrd has taught an arbitration module operably coupled to the control block and the second operation unit, wherein the arbitration module receives operation codes from a plurality of thread controllers corresponding to the plurality of threads, wherein the arbitration module determines order of execution of the operation codes received (Byrd page 39). A person of ordinary skill in the art, and as taught in Byrd, would recognize that multi-threading is best suited for scientific and engineering programs (Byrd page 38) and increases the speed and efficiency in the processor by allowing the processor to run other procedures while waiting for a longer background operations, such as accessing slower memory, to complete (Byrd pages 38-40). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multi-threading of Byrd in the device of Alidina to increase speed and decrease processor idle time.

12. Referring to claim 8, Alidina has taught wherein the accumulation circuit is included in a vector engine that performs at least one of dot product operations, vector multiply accumulate operations, vector addition operations, and vector multiplication operations (Alidina column 2, lines 57-60). Alidina has not taught multi-threading. However, Alidina has taught a digital signal processor specializing in scientific calculations (Alidina column 1, lines 17-28). Byrd has taught multi-threading (Byrd pages 38-40). A person of ordinary skill in the art, and as taught in Byrd, would recognize that multi-threading is best suited for scientific and engineering programs (Byrd page 38) and increases the speed and efficiency in the processor by allowing the processor to run other procedures while waiting for a longer background operations, such as accessing

slower memory, to complete (Byrd pages 38-40). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multi-threading of Byrd in the device of Alidina to increase speed and decrease processor idle time.

13. Referring to claim 9, Alidina has taught a memory operably coupled to the selection block, the first operation unit, and the control block, wherein the memory stores the first operation result produced by the first operation unit, wherein contents of the memory are selectively included in the set of potential operands based on a portion of the control information generated by the control block (Alidina column 2, lines 12-19 and 46-48; columns 4-5, lines 26-7; and Figure 3).

14. Referring to claim 10, Alidina has taught wherein at least a portion of the plurality of accumulation registers include a first register section and a second register section, wherein the first register section is used for accumulation operations corresponding to a first set of operation codes and the second section is used for accumulation operations corresponding to a second set of operation codes (Alidina columns 1-2, lines 54-15 and Figure 1).

15. Referring to claim 12, Alidina has taught a method for performing a plurality of combine and accumulate operations, comprising:

a. Receiving a first set of operands, wherein the first set of operands corresponds to a first accumulation operation (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3)

b. Combining the first set of operands to produce a first result (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5; lines 26-7; and Figure 3)

c. Storing the first result in the selected accumulation register to produce a first accumulated value (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5; lines 26-7; and Figure 3)

d. Receiving a second set of operands corresponding to the selected thread, wherein the second set of operands corresponds to a second accumulation operation (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5; lines 26-7; and Figure 3)

e. Combining the second set of operands to produce a second result (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5; lines 26-7; and Figure 3)

f. Combining the second result with the first accumulated value to produce a second accumulated value (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5; lines 26-7; and Figure 3)

g. Storing the second accumulated value in the selected register to produce a second accumulated result (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5; lines 26-7; and Figure 3).

h. Selecting a selected accumulation register from a plurality of accumulation registers (Alidina column 1, line 64 to column 2, line 5)

16. Alidina has not taught multi-threading and having registers and operands which correspond to each individual thread. However, Alidina has taught a digital signal processor specializing in scientific calculations (Alidina column 1, lines 17-28). Byrd has taught multi-threading and having registers and operands which correspond to each individual thread (Byrd pages 38-40). A person of ordinary skill in the art, and as taught in Byrd, would recognize that

multi-threading is best suited for scientific and engineering programs (Byrd page 38) and increases the speed and efficiency in the processor by allowing the processor to run other procedures while waiting for a longer background operations, such as accessing slower memory, to complete (Byrd pages 38-40). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multi-threading of Byrd in the device of Alidina to increase speed and decrease processor idle time.

17. Referring to claim 13, Alidina has taught wherein combining the first set of operands includes combining the first set of operands using a multiplication operation, and wherein the combining the second set of operations further comprises combining the second set of operands using a multiplication operation (Alidina column 2, lines 46-481 columns 4-5, lines 26-7; and Figure 3).

18. Referring to claim 14, Alidina has taught wherein combining the second result with the first accumulated value further comprises combining the second result with the first accumulated value using an addition operation such that a multiply and accumulate operation for the first and second sets of operands is achieved (Alidina column 2, lines 46-65).

19. Referring to claim 15, Alidina has taught the method comprises:

a. Receiving subsequent sets of operands corresponding to subsequent accumulation operations (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3);

b. For each subsequent set of operands:

i. Combining the subsequent set of operands to produce a subsequent result (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3)

ii. Combining the subsequent result with a current value stored in the selected accumulation register to produce a subsequent accumulated result (Alidina Abstract, lines 1-4; columns 1-2, lines 64-5; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3)

iii. Storing the subsequent accumulated result in the selected accumulation register such that the current value stored in the selected accumulation register is updated (Alidina Abstract, lines 1-4; columns 1-2, lines 64-5; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3).

20. Alidina has not taught multi-threading and having registers and operands which correspond to each individual thread. However, Alidina has taught a digital signal processor specializing in scientific calculations (Alidina column 1, lines 17-28). Byrd has taught multi-threading and having registers and operands which correspond to each individual thread (Byrd pages 38-40). A person of ordinary skill in the art, and as taught in Byrd, would recognize that multi-threading is best suited for scientific and engineering programs (Byrd page 38) and increases the speed and efficiency in the processor by allowing the processor to run other procedures while waiting for a longer background operations, such as accessing slower memory, to complete (Byrd pages 38-40). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multi-threading of Byrd in the device of Alidina to increase speed and decrease processor idle time.

21. Referring to claim 16, Alidina has taught performing combination operations subsequent to combining the first set of operands and prior to combining the second set of operands (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3). Alidina has not taught the operations corresponding to at least one additional thread of the plurality of threads. However, Alidina has taught a digital signal processor specializing in scientific calculations (Alidina column 1, lines 17-28). Byrd has taught the operations corresponding to at least one additional thread of the plurality of threads (Byrd pages 38-40). A person of ordinary skill in the art, and as taught in Byrd, would recognize that multi-threading is best suited for scientific and engineering programs (Byrd page 38) and increases the speed and efficiency in the processor by allowing the processor to run other procedures while waiting for a longer background operations, such as accessing slower memory, to complete (Byrd pages 38-40). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multi-threading of Byrd in the device of Alidina to increase speed and decrease processor idle time.

22. Referring to claim 17, Alidina has taught a multi-thread multiply and accumulate circuit, comprising:

a. A multiplier operably coupled to the arbitration module, wherein the multiplier combines a set of operands corresponding to each command code being executed to produce a product from which the command code being executed originated (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3)

b. An adder operably coupled to the multiplier, wherein the adder combines the product of the multiplier with a second operand that is received to produce a sum (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3)

c. A plurality of accumulation registers operably coupled to the adder, wherein each of the plurality of accumulation registers (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3)

d. A selection block operably coupled to the plurality of accumulation registers and the adder, wherein the selection block selects the second operand from a set of potential operands based on control information derived from the command code being executed, wherein the set of potential operands includes values stored in each of the plurality of accumulation registers (Alidina column 4, lines 63-66 and Figure 3, element SMUX).

e. Wherein a selected accumulation register stores the sum corresponding to the selected thread

f. Wherein at least a portion of the command codes correspond to multiply and accumulate operations (Alidina column 5, lines 8-18).

23. Alidina has not taught multi-threading and having registers and operands which correspond to each individual thread. However, Alidina has taught a digital signal processor specializing in scientific calculations (Alidina column 1, lines 17-28). Byrd has taught multi-threading and having registers and operands which correspond to each individual thread (Byrd pages 38-40). A person of ordinary skill in the art, and as taught in Byrd, would recognize that

multi-threading is best suited for scientific and engineering programs (Byrd page 38) and increases the speed and efficiency in the processor by allowing the processor to run other procedures while waiting for a longer background operations, such as accessing slower memory, to complete (Byrd pages 38-40). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multi-threading of Byrd in the device of Alidina to increase speed and decrease processor idle time.

24. In addition, Alidina has not explicitly taught an arbitration module that receives command codes corresponding to a plurality of threads, wherein the arbitration module determines an order of execution of the command codes. However, Alidina has taught a digital signal processor specializing in scientific calculations (Alidina column 1, lines 17-28). Byrd has taught an arbitration module that receives command codes corresponding to a plurality of threads, wherein the arbitration module determines an order of execution of the command codes (Byrd pages 39). A person of ordinary skill in the art, and as taught in Byrd, would recognize that multi-threading is best suited for scientific and engineering programs (Byrd page 38) and increases the speed and efficiency in the processor by allowing the processor to run other procedures while waiting for a longer background operations, such as accessing slower memory, to complete (Byrd pages 38-40). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multi-threading of Byrd in the device of Alidina to increase speed and decrease processor idle time.

25. Referring to claim 18, Alidina has taught wherein the set of potential operands includes at least one additional operand, wherein the at least one additional operand is at least one of a constant, a state variable, and data stored in a memory structure as a result of previous operations

performed by the circuit (Alidina column 2, lines 12-19 and 46-48; columns 4-5, lines 26-7; and Figure 3).

26. Referring to claim 19, Alidina has taught wherein at least a portion of the plurality of accumulation registers include a first register section and a second register section, wherein the first register section is used for accumulation operations corresponding to a first set of operation codes and the second section is used for accumulation operations corresponding to a second set of operation codes (Alidina columns 1-2, lines 54-15 and Figure 1).

27. Referring to claim 21, Alidina has taught an accumulation circuit that supports a plurality of threads, comprising:

a. A first operation unit operably coupled to receive a first operand and a second operand corresponding to an operation code issued, wherein the operation unit combines the first and second operands to produce a first operation result (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3)

b. A plurality of accumulation registers operably coupled to the first operation unit, wherein each accumulation register of the plurality of accumulation registers (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3, element 30)

c. A selection block operably coupled to the plurality of accumulation registers and the first operation unit, wherein the selection block selects the second operand provided to the first operation unit from a set of potential operands, wherein the set of potential operands includes contents of each accumulation register of the

plurality of accumulation registers (Alidina column 4, lines 63-66 and Figure 3, element SMUX).

d. Wherein a selected accumulation register stores the first operation result (Alidina column 1, line 64 to column 2, line 5)

28. Alidina has not taught

a. Multi-threading and having registers and operands which correspond to each individual thread; and

b. Wherein when the operation code is dependent on the results of a previously issued operation code, the selection block will not release the dependent operation code until a predetermined amount of time has passed corresponding to the latency associated with executing the previously issued operation code.

29. However, Alidina has taught a digital signal processor specializing in scientific calculations (Alidina column 1, lines 17-28). Byrd has taught

a. Multi-threading and having registers and operands which correspond to each individual thread (Byrd pages 38-40); and

b. Wherein when the operation code is dependent on the results of a previously issued operation code, the selection block will not release the dependent operation code until a predetermined amount of time has passed corresponding to the latency associated with executing the previously issued operation code (Byrd pages 38-40, 42, and 45-46).

30. A person of ordinary skill in the art, and as taught in Byrd, would recognize that multi-threading is best suited for scientific and engineering programs (Byrd page 38) and increases the

speed and efficiency in the processor by allowing the processor to run other procedures while waiting for a longer background operations, such as accessing slower memory, to complete (Byrd pages 38-40). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multi-threading of Byrd in the device of Alidina to increase speed and decrease processor idle time.

31. Referring to claim 22, Alidina has taught a control block operably coupled to the selection block and the plurality of accumulation registers, wherein the control block receives information based on the operation code and generates control information provided to the plurality of accumulation registers and the selection block, wherein the control information provided to the plurality of accumulation registers causes the selected accumulation register to store the result when the operation code corresponds to an accumulate operation (Alidina column 5, lines 8-18). Alidina has not taught multi-threading and having registers and operands which correspond to each individual thread. However, Alidina has taught a digital signal processor specializing in scientific calculations (Alidina column 1, lines 17-28). Byrd has taught multi-threading and having registers and operands which correspond to each individual thread (Byrd pages 38-40). A person of ordinary skill in the art, and as taught in Byrd, would recognize that multi-threading is best suited for scientific and engineering programs (Byrd page 38) and increases the speed and efficiency in the processor by allowing the processor to run other procedures while waiting for a longer background operations, such as accessing slower memory, to complete (Byrd pages 38-40). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multi-threading of Byrd in the device of Alidina to increase speed and decrease processor idle time.

32. Claims 11 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alidina et al., U.S. Patent Number 6,446,193 (herein referred to as Alidina) in view of Gregory T. Byrd and Mark A. Holliday's "Multithreaded Processor Architectures" ©1995 (herein referred to as Byrd) as applied to claims 10 and 19 above, and further in view of Berkaloff, U.S. Patent Number 5,673,377 (herein referred to as Berkaloff).

33. Referring to claim 11, Alidina has not explicitly taught wherein the first register section accumulates diffuse color information corresponding to graphics primitives, and wherein the second register section accumulates specular color information corresponding to the graphics primitives. However, Alidina has taught that DSP processors are optimal for certain graphical and audio operations requiring multiplication, accumulation, and other processor intensive operations. Berkaloff has taught that diffuse and specular color information is needed for 3-D graphical calculations (Berkaloff column 1, lines 17-59). It would have been obvious to one of ordinary skill in the art to incorporate the color information of Berkaloff, because it is needed in the calculations to create effective images. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the color information of Berkaloff in the device of Alidina.

34. Referring to claim 20, Alidina has not explicitly taught wherein the first register section accumulates diffuse color information corresponding to graphics primitives, and wherein the second register section accumulates specular color information corresponding to the graphics primitives. However, Alidina has taught that DSP processors are optimal for certain graphical and audio operations requiring multiplication, accumulation, and other processor intensive operations. Berkaloff has taught that diffuse and specular color information is needed for 3-D

graphical calculations (Berkaloff column 1, lines 17-59). It would have been obvious to one of ordinary skill in the art to incorporate the color information of Berkaloff, because it is needed in the calculations to create effective images. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the color information of Berkaloff in the device of Alidina.

Response to Arguments

35. Applicant's arguments filed 09 August 2004 have been fully considered but they are not persuasive.

36. Applicant argues on page 10 in essence,

> "...the Office Action fails to show where the combination of Alidina and Byrd teach 'wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread.'...does not specifically show how Byrd as cited, teaches 'wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread.'"

37. This has not been found persuasive. Alidina's Figure 3 shows accumulation registers in element 30 which store results from the ALU, ADD, or BMU operations units via the SMUX. Byrd was combined to teach the multiple thread and saving data and information, like the accumulation register, of a thread (Byrd pages 38-40). It is the combination of these two references which teaches the claims of the current application. Not one of them teaches all aspects of the invention. To argue that Byrd does not teach the claim or to argue that Alidina does not teach the claim does not reflect that a 103(a) combination rejection was made. Each

reference teaches a specific aspect of the invention, as shown in the above rejection. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

38. Applicant argues in essence on pages 11-12 and 14 "...Alidina, is directed to a problem different from that addressed in the claims." This has not been found persuasive. In response to applicant's argument that Alidina solves a different problem from the current application, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

39. Applicant argues in essence on pages 13-14 "...Fig. 3 fails to show the specific routing path, and, further, failed to show the required control signals to establish any such path..." This has not been found persuasive. Alidina's Figure 3 spans two pages and is easier to understand when the two pages are held vertically aligned with Fig. 3 (cont.) on the bottom. The dotted outlines on the bottom of the Fig. 3 page represent MUX1, MUX2, and MUX3 and the dotted lines represent the connections that cross the pages. The outputs from the accumulation registers 30 have connections following along the side of the page to the first Fig. 3. These connections are inputs to MUX1, MUX2, and MUX3, which control the inputs to the ALU, ADD, and BMU

operation units. Figure 3 also shows that the output connections on the right side feed directly into the ADD and BMU units. There are also other inputs connected to the ALU, ADD, and BMU units shown in Figure 3. These units operate on these inputs to produce results that are then fed into the accumulation registers 30 via SMUX, which chooses the correct output to feed.

40. Applicant's argue in essence on pages 15-17 "Neither Alidina nor Wilson teaches..." This has not been found persuasive. The rejection was Alidina in view of Byrd, as shown in the above rejection. Alidina was used to show the components of a typical digital signal processor, such as the accumulation registers, operational units, and selectors, while Byrd was used to show the benefits of incorporating multi-threading and having corresponding registers for each thread. Please see the rejection above for more information.

41. Applicant's argue in essence on pages 17-18 "...the motivation provided...to combine the references...provide no basis for the meaning of 'effective images,' and further uses circular reasoning, and therefore fails to establish motivation to combine the references." This has not been found persuasive. The specular color information is needed for 3-D rendering of images, specifically as part of the shading parameters. The shading parameters are needed for a computer device to render the 3-D appearance, i.e. make a recognizable, or effective, image. In particular, without the shading in a 3-D image it is difficult to see the 3-D nature, since the shadows which accent the 3-D nature are no longer present in the image.

Conclusion

42. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

43. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

44. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

45. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

46. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL

Aimee J. Li
15 November 2004

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